REMARKS/ARGUMENTS

Claims 1-20 are pending in this application. The Office Action, dated February 3, 2005: rejected claims 1-4, 6, and 10-15 under 35 USC § 102(b), rejected claims 1-4, 6, and 11-15 under 35 USC § 103(a), and objected to claims 5, 7-10, and 16-20 as based on a rejected base claim but are otherwise allowable, and accepted the drawings filed on November 15, 2004. Applicant thanks the Examiner for the review and indication of allowable subject matter for claims 5, 7-10 and 16-20. Claims 13-20 are amended, not to overcome any basis of rejection, but merely to correct for a minor infelicity. The objections and rejections are believed to be overcome for the reasons stated below. No new matter is added.

Drawings

The office action stated that the drawings filed on November 15, 2004 are accepted with objections made as to Figs. 1A and 1B. In particular, Figs. 1A and 1B are requested to be amended to include the designation "Prior Art". Replacement sheets for Figs 1A and 1B are hereby submitted in accordance with the Examiner's request, and it is kindly requested that the objection to the drawings be withdrawn.

Rejection of Claims 1-4, 6, and 10-15 under 35 USC § 102(b)

Claims 1-4, 6, and 10-15 are rejected under 35 USC § 102(b) as being anticipated by Torikoshi et al. (US Patent No. 5,436,614). In particular, the office action notes that the Figs. 1 and 4 of the Torikoshi reference discloses: "an integrated circuit comprising a PTAT voltage temp sensor block 19, a level shifter block R4/Q providing a level shifted signal V(-), a gain block SW/R1-R3/OP with a gain providing an output signal A/D, an ADC A/D and a central

logic block CPU providing a control signal to SW as recited in claims 1-3, 10 and 11." Alternatively, the office action states that Figs. 1 and 7a/b of the Torikoshi reference discloses: " an integrated circuit comprising a PTAT voltage temp sensor block 19, a level shifter block (R4 & switches) providing a level shifted signal to a gain block Q with a gain providing an output signal A/D, an ADC A/D and a central logic block CPU providing a control signal to switches as recited in claims 1-3, 10 and 11." The above stated rejections to claims 1-4, 6, and 10-15 under 35 USC § 102(b) are traversed for the reasons that follow below.

Applicant's claim 1 includes at least the following limitations that are not found in the cited prior art references:

> "**a level shifter block** that is arranged to: receive the temperature signal (TEMP), and provide **a level shifted temperature signal** (TEMPLS) that is **related to** the temperature signal (TEMP) **by a DC level shift**"
>
> "**a gain block** that is arranged to: **receive the level shifted temperature signal** (TEMPLS) and **provide an output signal** (OUT) that is **related to** the level shifted temperature signal (TEMPLS) according to **a gain factor** (G)"
>
> and
>
> "**a control logic block** that is **arranged to: receive the control signal (CTL2)** and **provide another control signal (CTL1) to at least one of the level shifter block and the gain block** such that a **dynamic range** associated with the temperature sensitivity of the apparatus is extended."

The Torikoshi reference does not teach nor disclose each of the recited structural elements that are found in applicants claim 1. Instead, the Torikoshi reference (see col. 4, lines 23 - 25) teaches that a constant current source (18) is series connected to a thermistor (19) to

operate as a thermal sensor that provides a voltage to the A/D converter (17). The temperature sensor that is illustrated in FIGS. 1-7a/b is not merely the thermistor, which is essentially a resistance that varies with respect to temperature. In fact, the thermistor alone is incapable of generating a signal without the current that is provided by the constant current source. At most, the Toriskkoshi reference teaches that the bias current to the thermistor (which is actually a necessary **part** of the temperature sensor) may be varied to change the operation of the actual sensor. In contrast, Applicant's claim 1 describes that the "level shifter block ... receive(s) the temperature signal" and "provide(s) a level shifted temperature signal ... that is related ... by a DC level shift."

Moreover, the circuits described with respect to Figs. 4-7a/b of the Torikoshi reference are merely variations of the constant current source implementation that is necessary to bias the thermistor. For example, Fig. 4 illustrates an operational amplifier (OP) that is arranged to sense a reference voltage at its non-inverting input terminal (+), and control a current delivered to the base of transistor (Q) such that the inverting input terminal (-) is matched to the reference voltage and such that the current that is provided to the thermistor is temperature insensitive. The combination of Figs. 1 and 4 merely places the constant current circuit and thermistor into the system that connects the output of the temperature sensor (18 and 19) to the A/D converter (17).

Figs. 5 - 7a/b add no further guidance and are merely variations on achieving the same theme, which is changing the operating range of the temperature sensor by adjusting the operating current for the thermistor. For example, Figs. 7a/b illustrates that the selection of the constant current can be changed from base side of transistor Q (as is illustrated by Figs. 4-6) to

varying the selection of the constant current on the emitter side of transistor Q (via switching the selection of resistor R4). However, the resulting temperature sensor still has a constant current that biases the thermistor similar to that described with respect to Figs. 1 and 4.

Figs. 4-7a/b also do not teach the gain feature that is described in Applicant's claim 1. Referring to Fig. 2 and col. 4, lines 36-40 of Torikoshi, the temperature sensor is biased at a different operating current (e.g., I1, I2, I3) that are constant. Since constant current is provided to the thermistor, which has a linear response with respect to temperature, the gain of the temperature response is also a constant. This lack of gain adjustment is illustrated, for example, by the constant slope curves illustrated in Fig. 2.

Each of the Figures and accompanying text in the Torikoshi reference describes variations on the same circuit topology: an adjustable biasing current for the thermistor that is found within the temperature sensor. Since the Torikoshi reference does not teach the level shifter and gain blocks as described in Applicant's claim 1, the further structural and functional limitations of Applicant's claim 1 cannot be met. For example, the "analog-to-digital converter" of Applicant's claim 1 is arranged to receive the output signal, which is provided from the "gain block." Since no gain block exists that satisfies Applicant's claim 1, then how can the analog-to-digital converter receive its output? Similarly, the "control logic block" of Applicant's claim 1 receives the control signal from the analog-to-digital converter block and provides another control signal to at least one of the level shifter block and the gain block. How can a gain block and a level shifter block be controlled if they don't exist?

For at least the reasons stated above, it is respectfully submitted that the Torikoshi reference does not anticipate applicant's claim 1 and claim 1 is believed to be in proper form for allowance. Applicant's claims 2-4, 10 and 11 depend upon and further limit claim 1, and are proposed to be allowable for that reason as well as any additional limitations they recite. It is requested that the rejection of claims 1-4, 10 and 11 under 35 USC § 102(b) be withdrawn and that notice to that effect be provided. Claims 12 - 15 are believed to be allowable for those reasons previously discussed above, and notice to that effect is requested.

Rejection of Claims 1-4, 6, and 11-15 under 35 USC § 103(a)

Claims 1-4, 6, and 11-15 are rejected under 35 USC § 103(a) as being unpatentable over Hara et al. (US Patent No. 5,140,302) in view of McCormack (US Patent No. 3,790,910). The office action states that Fig. 1 of Hara discloses "an integrated circuit comprising a PTAT voltage temp sensor block 1, a level shifter block R1-R3/Q1 providing a level shifted signal, an ADC 2b and a central logic block 2a providing a control signal to Q1", and that Hara "does not appear to disclose the gain block recited in claim 1. The office action further states that McCormack discloses a similar circuit including gain block 50, and that "it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the Hara et al. circuit with a gain block as taught by McCormack for the benefit of isolating the ADC from the temp and level shifter blocks." The office action further states that claims 1-3 and 11 are obvious, and that Frazier and Nakamura also teach the benefits of using gain blocks to isolate ADCs from preceding block. Applicant's respectfully traverse this rejection as follows below.

Figs. 1 and 2 of the Hara reference illustrate a temperature sensor that includes a water temperature sensor (1) that is represented as a resistor, and an adjustable biasing circuit (R1 - R3/R3 and Q1) for the water temperature sensor. The equivalent circuit for the biasing circuit is a current source that provides a biasing current to the water temperature sensor (1). For example, water temperature sensor (1) does not provide an output signal unless biased by a biasing current that is provided by resistors R1 and R2. As illustrated by Figs. 1 and 2, the resistance of R1 can be decreased by switching in resistor R3, and the resistance of R2 can be decreased by switching in resistor R4 as is illustrated in Figs. 1 and 2. Since the effective circuit that results is still an adjustable biasing circuit that biases the temperature sensor (1), the same arguments that were described with respect to the Torikoshi reference are applicable to the Hara reference. Namely, the Torikoshi reference does not teach level shifting the output of the temperature sensor, and instead teaches changing the temperature sensors operation through biasing.

The McCormack reference does not cure the ails of the Hara reference since neither reference separately nor combined teaches that: an output from a temperature sensor is coupled to a level shifter block, whose output is coupled to a gain block, where the output of the gain block is coupled to an A/D converter block, and where the output of the A/D converter block is coupled to a control logic block that controls at leasts one of the level shifter block and the gain block for extended dynamic range. Although the office action states that and that "it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the Hara et al. circuit with a gain block as taught by McCormack for the benefit of isolating the ADC from the temp and level shifter blocks.", the isolation of the ADC from the temp and level shifter blocks does not result in the Applicant's invention as claimed in claims 1-4, 6, and 11-15. The

further note that the Frazier and Nakamura references "teach the benefits of using gain blocks to isolate ADCs from preceding blocks" does not add any further guidance, teachings or suggestions that would result in the Applicant's invention. It is only with the benefit of impermissible hindsight reconstruction that the cited references can be modified to provide the Applicant's claimed invention.

Since not all of the claim elements are found in the cited prior art references without reengineering the circuits with the benefit of hindsight reconstruction, it is believed that the rejection of the claims under 35 USC §103(a) is properly traversed. Claims 1-4, 6 and 11-15 are proposed to be allowable for the reasons discussed above, and a notice to that effect is requested.

In view of the foregoing amendments and remarks, all pending claims are believed to be allowable and the application is in condition for allowance. Therefore, a Notice of Allowance is respectfully requested. Should the Examiner have any further issues regarding this application, the Examiner is requested to contact the undersigned attorney for the applicant at the telephone number provided below.

Respectfully submitted,

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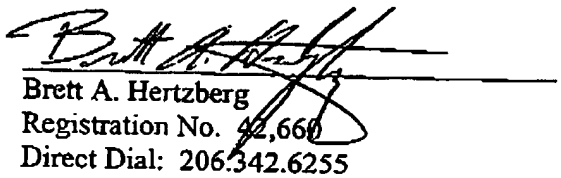

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